ANALOG DEVICES

3 V to 5 V Single Supply, 600 kSPS 12-Bit Sampling ADCs

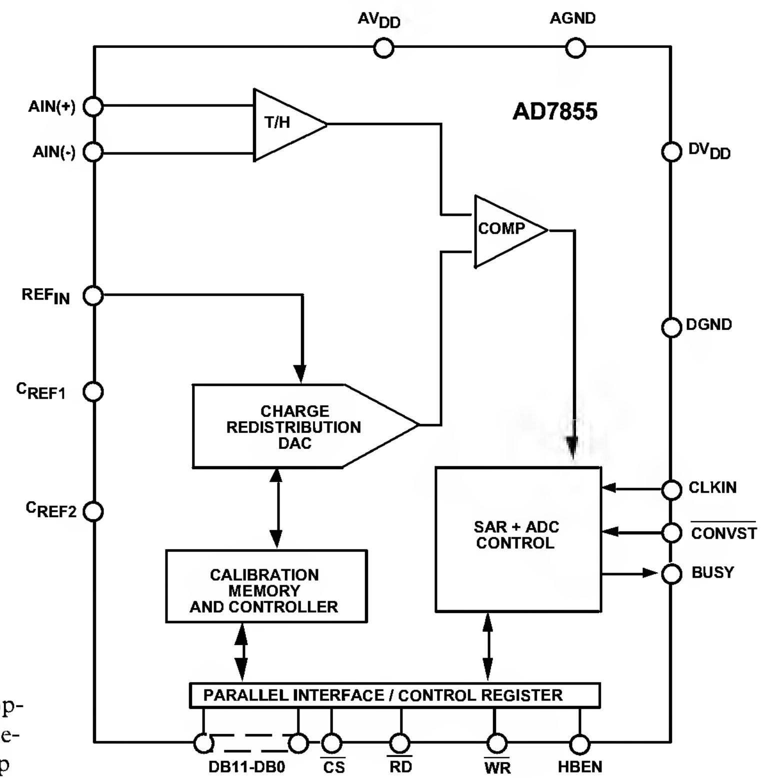
Preliminary Technical Data — AD7855

FEATURES
Specified for V_{DD} of 3 V to 5.5 V
Read-Only Operation
System and Self-Calibration

Flexible Parallel Interface
12-Bit Parallel/8-Bit Parallel
28-Pin SOIC and SSOP Packages

APPLICATIONS
Instrumentation and Control Systems
High Speed Modems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7855 is a high speed, low power, 12-bit ADC that operates from a single 3 V or 5 V power supply, the AD7855 being optimized for speed and low power. The ADC powers up with a set of default conditions at which time it can be operated as a read-only ADC. The ADC contains self-calibration and system calibration options to ensure accurate operation over time and temperature and has a number of power-down options for low power applications.

The AD7855 is capable of 600 kHz throughput rate . The input track-and-hold acquires a signal in 500 ns and features a pseudo-differential sampling scheme. The AD7855 input voltage range is 0 to V_{REF} (unipolar) and $-V_{REF}/2$ to $+V_{REF}/2$, centered at $V_{REF}/2$ (bipolar). The coding is straight binary in unipolar mode and twos complement in bipolar mode. Input signal range is to the supply and the part is capable of converting full-power signals to 400 kHz.

CMOS construction ensures low power dissipation . The part is available in 28-pin small outline (SOIC) and 28-lead small shrink outline (SSOP) packages.

PRODUCT HIGHLIGHTS

1. Operation with either 3 V or 5 V power supplies.
2. Flexible power management options including automatic power-down after conversion. By using the power management options a superior power performance at slower throughput rates can be achieved:
3. Operates with reference voltages from 1.2 V to AV_{DD}.
4. Analog input ranges from 0 V to AV_{DD}.
5. Self-calibration and system calibration.
6. Versatile parallel I/O port.

Prelim A 12/97

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AD7855–SPECIFICATIONS[1, 2]

($AV_{DD} = DV_{DD} = +3.0$ V to $+5.5$ V, $REF_{IN} = 2.5$ V External Reference, $f_{CLKIN} = 12$ MHz ; $f_{SAMPLE} = 600$ kHz ; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Signal to Noise + Distortion Ratio[3] (SNR)	70	dB min	Typically SNR is 72 dB V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 600 kHz
Total Harmonic Distortion (THD)	–78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 600 kHz
Peak Harmonic or Spurious Noise	–78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 600 kHz
Intermodulation Distortion (IMD)			
Second Order Terms	–78	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 600 kHz
Third Order Terms	–78	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 600 kHz
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity	±1	LSB max	5 V Reference V_{DD} = 5 V
Differential Nonlinearity	±1	LSB max	Guaranteed No Missed Codes to 12 Bits
Unipolar Offset Error	±3	LSB max	
	±2	LSB typ	
Unipolar Gain Error	±4	LSB max	
	±2	LSB typ	
Bipolar Positive Full-Scale Error	±4	LSB max	
	±2	LSB typ	
Negative Full-Scale Error	±4	LSB max	
	±2	LSB typ	
Bipolar Zero Error	±4	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{REF}	Volts	i.e., AIN(+) – AIN(–) = 0 to V_{REF}, AIN(–) can be biased up but AIN(+) cannot go below AIN(–).
	$\pm V_{REF}/2$	Volts	i.e., AIN(+) – AIN(–) = $-V_{REF}/2$ to $+V_{REF}/2$, AIN(–) should be biased to $+V_{REF}/2$ and AIN(+) can go below AIN(–) but cannot go below 0 V.
Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT			
REF_{IN} Input Voltage Range	$2.3/V_{DD}$	V min/max	Functional from 1.2 V
Input Impedance	150	kΩ typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	3	V min	$AV_{DD} = DV_{DD}$ = 4.5 V to 5.5 V
	2.1	V min	$AV_{DD} = DV_{DD}$ = 3.0 V to 3.6 V
Input Low Voltage, V_{INL}	0.4	V max	$AV_{DD} = DV_{DD}$ = 4.5 V to 5.5 V
	0.6	V max	$AV_{DD} = DV_{DD}$ = 3.0 V to 3.6 V
Input Current, I_{IN}	±10	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}			I_{SOURCE} = 200 µA
	4	V min	$AV_{DD} = DV_{DD}$ = 4.5 V to 5.5 V
	2.4	V min	$AV_{DD} = DV_{DD}$ = 3.0 V to 3.6 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 0.8 mA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[4]	10	pF max	
Output Coding	Straight (Natural) Binary		Unipolar Input Range
	Twos Complement		Bipolar Input Range
CONVERSION RATE			t_{CLKIN} x 18
Conversion Time	1.2	µs max	
Track/Hold Acquisition Time	0.5	µs min	

Parameter	A Version[1]	Units	Test Conditions/Comments
POWER REQUIREMENTS			
AV_{DD}, DV_{DD}	+3.0/+5.5	V min/max	
I_{DD}			
Normal Mode[5]	15	mA max	$AV_{DD} = DV_{DD}$ = 3.0 V to 5.5 V. Typically 12 mA
Sleep Mode[6]			
With External Clock On	10	µA typ	Full power-down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 0.
	400	µA typ	Partial power-down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 1.
With External Clock Off	5	µA max	Typically 1 µA. Full power-down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 0.
	200	µA typ	Partial power-down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 1.
Normal Mode Power Dissipation	75	mW max	V_{DD} = 5.5 V: Typically 55 mW
	45	mW max	V_{DD} = 3.6 V: Typically 30 mW
Sleep Mode Power Dissipation			
With External Clock On	55	µW typ	V_{DD} = 5.5 V
	36	µW typ	V_{DD} = 3.6 V
With External Clock Off	27.5	µW max	V_{DD} = 5.5 V: Typically 5.5 µW
	18	µW max	V_{DD} = 3.6 V: Typically 3.6 µW
SYSTEM CALIBRATION			
Offset Calibration Span[7]	$+0.05 \infty V_{REF}/-0.05 \infty V_{REF}$		V max/min Allowable Offset Voltage Span for Calibration
Gain Calibration Span[7]	$+0.025 \infty V_{REF}/-0.025 \infty V_{REF}$		V max/min Allowable Full-Scale Voltage Span for Calibration

NOTES
[1]Temperature range –40°C to +85°C.
[2]Specifications apply after calibration.
[3]Not production tested. Guaranteed by characterization at initial product release.
[4]Sample tested @ +25°C to ensure compliance.
[5]All digital inputs @ DGND except for $\overline{\text{CONVST}}$ @ DV_{DD}. No load on the digital outputs. Analog inputs @ AGND.
[6]CLKIN @ DGND when external clock off. All digital inputs @ DGND except for $\overline{\text{CONVST}}$ @ DV_{DD}. No load on the digital outputs. Analog inputs @ AGND.
[7]The offset and gain calibration spans are defined as the range of offset and gain errors that the AD7855 can calibrate. Note also that these are voltage spans and are not absolute voltages (i.e., the allowable system offset voltage presented at AIN(+) for the system offset error to be adjusted out will be AIN(–) $\pm 0.05 \infty V_{REF}$, and the allowable system full-scale voltage applied between AIN(+) and AIN(–) for the system full-scale voltage error to be adjusted out will be $V_{REF} \pm 0.025 \infty V_{REF}$ (unipolar mode) and $V_{REF}/2 \pm 0.025 \infty V_{REF}$ (bipolar mode)). This is explained in more detail in the calibration section of the data sheet.

Specifications subject to change without notice.